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10/807,542	03/23/2004	Yusuke Ota	9319S-000700	3775

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EXAMINER	
SHAPIRO, LEONID	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/807,542	OTA, YUSUKE	
	Examiner	Art Unit	
	Leonid Shapiro	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 July 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3 and 5-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3 and 5-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1, 3, 5-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akimoto et al., United States Patent Number US 6,856,308 B2 (hereinafter referred to as "Akimoto '308").

1. With regard to claim 1, Akimoto '308 clearly teaches **a display driver for driving data lines of an electro optic device based on display data** (see FIG. 1 generally and further described at column 4, lines 1-37) **comprising: a display data random access memory** (see FIGs 1 and 2 disclosing an SRAM frame memory 7 further described at column 5, lines 45-end) **including a plurality of word lines** (see FIG. 2 element 22 and column 5, lines 46-50)**, a plurality of column lines** (see column 5, lines 50-60 describing data lines 26 further see FIG. 2 element 26)**, and a plurality of memory cells each storing display data of one pixel** (see FIG. 2, element 21, further described in column 5, lines 46-48)**; a display address decoder selecting a word line of the display data random access memory based on a display address** (see column 5, lines 60-65, describing X decoder 31 further illustrated in FIG. 2)**; a display column address decoder selecting a column line of the display data random access memory based on a display column address** (see FIG. 2, further described in column 5, lines 49-50, Y decoder 23)**; a plurality of read-out bit lines each**

commonly coupled to a memory cell group specified by a corresponding column line (see FIG. 2, and further descried at column 6, lines 30-44)**; a scroll bus coupled to the plurality of read-out bit lines** (see FIG. 1, bus 18 further described at column 6, lines 45-48)**; a shift register outputting a shift output shifted based on a given shift clock** (see FIG. 1 further described in column 4, lines 25-30, 43-65 describing shift register 4, based on control signal)**, a plurality of shift register latches** outputting a plurality of shift outputs shifted (see FIG. 10, items 80-85, from col. 8, line 43 to col. 9, line 5)**; a plurality of data latches, each of which corresponds to one of the data lines of the electro optic device** (see FIG. 10, second latch circuit element 85, further described in column 8, lines 52-55)**, the plurality of data latches loading display data on the scroll bus** (see column 8, lines 55-60 describing element 79)**, one of plurality of the data latches coupled to the plurality of shift register latches** (see FIG. 10 and further describe in column 8, lines 43-60)**; and a driving circuit driving the data lines based on the display data loaded in the plurality of data latches** (see FIG. 11. describing driving operation of DA converter 11 at column 9, lines 10-30)**; display data of one pixel being read out from a memory cell specified by a word line selected by the display address decoder and a column line selected by the display column address decoder** (see FIG. 14 and further column 15, lines 9-42)**, the display data of one pixel being output to the scroll bus via the read-out bit line coupled to the memory cell** (see FIG.14 and further column 14, line 49-57 and additionally at column 15, lines 9-42, alternatively described at column 6, lines 45-52)**, the display data of one pixel on the scroll bus being loaded in each of the plurality of data latches**

(see FIG. 14, further at column 15, lines 30-43, and alternatively described at column 6, lines 31-end) **the display data of one pixel being shifted from the scroll bus for storing in the plurality of data latches** (see at least column 6, lines 45-end and FIG. 14)**, and one of the plurality of data latches loads display data on the scroll bus on one of the plurality of shift output** (see column 6, lines 31-end and further continued at column 7 lines 1-3).

Akimoto '308 does not disclose a given shift clock.

Akimoto '308 teaches that TCON 14 controls line memory 12 (fig. 1, col. 4, lines 5-38).

It would have been obvious to one of ordinary skill in the art at the time of the invention that control of line memory including shift register based on data shift clock in order to display an image (col. 1, lines 5-7 in the Akimoto '308 reference).

2. With regard to claim 3, Akimoto '308 in view of Oka '200 clearly teaches **the display driver according to claim 1** (see above)**, the driving circuit driving the data lines based on display data loaded in the line latches instead of the plurality of data latches** (see Akimoto '308 at column 6, lines 53-end)**.**

3. With regard to claim 5, Akimoto '308 in view of Oka '200 clearly teaches **an electro optic device** (see Akimoto '308 FIG.1 element 50)**, comprising: a plurality of scan lines** (see Akimoto '308, FIG. 1 at column 4, lines 5-15 gate line 3)**; a plurality of data lines** (see Akimoto '308, FIG. 1 at column 4, lines 10-20 describing signal line 5)**; a plurality of pixels coupled to the plurality of scan lines and the plurality of data lines** (see Akimoto '308 column 4, lines 5-10 describing a pixel cell 10)**; a scan driver**

scanning the plurality of scan lines (see Akimoto '308 describing gate line shift register 4, drives the gate lines 3 in conjunction with other elements)**; and the display driver according to claim 1 driving the plurality of data lines** (see claim 1 above)**.**

4. With regard to claim 6, Akimoto '308 in view of Oka '200 clearly teaches **an electro optic device** (see Akimoto '308 FIG.1 element 50)**, comprising: a display panel** (see Akimoto '308 column 4, lines 32-36 describing display panel) **including a plurality of scan lines** (see Akimoto '308, FIG. 1 at column 4, lines 5-15 gate line 3)**, a plurality of data lines** (see Akimoto '308, FIG. 1 at column 4, lines 10-20 describing signal line 5)**, and a plurality of pixels coupled to the plurality of scan lines and the plurality of data lines**(see Akimoto '308 column 4, lines 5-10 describing a pixel cell 10)**; a scan driver scanning the plurality of scan lines** (see Akimoto '308 describing gate line shift register 4, drives the gate lines 3 in conjunction with other elements)**; and the display driver according to claim 1 driving the plurality of data lines** (see claim 1 above)**.**

5. With regard to claim 7, Akimoto '308 in view of Oka '200 clearly teaches **an electronic apparatus, comprising: the electro optic device according to claim 5** (see above)**; and a display data generator generating display data to be supplied to the electro optic device** (see Akimoto '308 describing MUP 15 at but not limited to column 4, lines 42-65)**.**

6. With regard to claim 8, it is similarly analyzed as claim 1 above and rejected under the same rationale. The method for driving is similar to the display driver as described in claim 1.

7. With regard to claim 9, it is similarly analyzed as claim 3 above as dependent on claim 1 and rejected under the same rationale. The method of driving is similar to the display driver as described in claim 1.

8. Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akimoto et al., United States Patent Number US 6,856,308 B2 (hereinafter referred to as "Akimoto '308") as applied to claims 1 and 8 above respectively, and further in view of Oka et al., United States Patent Number 4,600,200 (hereinafter referred to as "Oka '200").

9. Regarding claim 10, Akimoto '308 clearly teaches the display driver for driving data lines of an electro optic device based on display data according to Claim 1, but does not explicitly teach **an image generated by loading the said display data being scrolled in an oblique direction to upper right, upper left, lower right, and lower left by combining vertical scrolling and horizontal scrolling based on the data output to the scroll bus and based on the shift output of each stage of the shift register.**

10. In the same field of endeavor, Oka '200 clearly teaches **an image generated by loading said display data is scrolled in an oblique direction to upper right, upper left, lower right, and lower left by combining vertical scrolling and horizontal scrolling based on the data output to the scroll bus** (see Abstract generally and further described in column 2, lines 7-30 describing operation, and additionally in

column 4, lines 14-24) **and based on the shift output of each stage of the shift register** (see column 6, lines 21-37)**.**

11. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have been motivated to incorporate the scrolling system as taught by Oka '200 into the display system of Akimoto '308 because both are within the same field of endeavor and furthermore, Oka '200 improves processing of moving images and objects, a common goal with in the art (see Oka '200 at column 1, lines 48-55).

12. Claim 11 is similarly analyzed as claim 10 above and rejected under the same rationale.

Response to Arguments

13. Applicant's arguments filed 07/31/08 have been fully considered but they are not persuasive.

On page 8 Applicant argues that Akimoto is In Akimoto et al., a gate line shift register (shown as 4 in Figure 1) is connected to a gate line, not a data line of the display. Akimoto et al., Col. 4, Lines 10-11. As stated in Akimoto et al., "[t]he gate of the pixel switch 2 is connected to gate line shift register 4 through a gate line 3." Akimoto et al., Col. 4, Lines 10-11. In this way, the gate line shift register of Akimoto et al. does not provide a shift clock to a data latch.

Examiner respectfully disagrees with this assessment. As addressed above, Akimoto clearly teaches these limitations (fig. 10, items 81-88 and correspondent text).

In order to avoid redundancy of argument, these limitations will not be readdressed here.

Telephone inquire

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Shapiro whose telephone number is 571-272-7683. The examiner can normally be reached on 8 a.m. to 5 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe can be reached on 571-272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

11.14.08
/L. S./
Examiner, Art Unit 2629

/Richard Hjerpe/
Supervisory Patent Examiner, Art Unit 2629